REMARKS

Claims 26 and 33 are amended. Claims 26-37 and 48-53 are in the application for consideration.

The Title of the invention is allegedly defective for not being descriptive. Applicant disagrees. Further, the Examiner's suggested Title is even less descriptive than Applicant's last pending Title. Regardless, the Title is herein amended towards overcoming the Examiner's objection. Accordingly, withdrawal of the rejection in the light of the Title amendment herein is requested.

The undersigned appreciates the Examiner's clarification in the last action wherein it was essentially asserted that the Examiner interprets openings 62 and 64, at least in Fig. 8, as collectively constituting what Applicant recites as its well. Independent claim 26 has been amended herein to recite that one of the storage node electrodes is spaced laterally inward of the outline peripherally defined by the well. Support for the same is inherent in the Applicant's application as filed, for example in Figs. 11+. Each of the exemplary illustrated storage nodes 47/49 is spaced laterally inward from periphery 35 of well 34. Independent claim 33 is likewise amended to recite that the respective storage node containers are spaced laterally inward of the outline peripherally defined by the well, and is also supported by Figs. 11+. Lane et al. clearly neither discloses nor suggests such. Even accepting the Examiner's alleged position that openings 62 and 64 collectively define a well, both of the Lane et al.'s capacitor electrodes 70, as shown in Fig. 14, are received against the periphery defined by the alleged well, and therefore are not spaced laterally inward of the outline

peripherally defined by the well, as Applicant now recites. For at least this reason, Applicant's independent claims 26 and 33 should be allowed, and action to that end is requested.

Applicant's dependent claims should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. Action to that end is requested.

Respectfully submitted,

Dated: 2-13-03

By: _____
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/810,595
Filing Date ..... March 15, 2001
Inventor ..... Belford T. Coursey
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Yennhu B. Huynh
Attorney's Docket No. MI22-1660
Title: Memory Circuitry With Plurality of Capacitors Received Within an Insulative Layer Well (As Amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 3, 2002 OFFICE ACTION TO ACCOMPANY RCE FILING

In the Title

The title is amended as follows, underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Memory Circuitry With ~~Array Area And Peripheral Area~~ Plurality Of Capacitors Received Within An Insulative Layer Well

EV085427392

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

26. (Amended) Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the one well over the word lines, individual of the capacitors having a storage node electrode, one of the storage node electrodes being spaced laterally inward of the outline peripherally defined by the well; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

33. (Amended) Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the one well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base, the respective storage node containers being spaced laterally inward of the outline peripherally defined by the well; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

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